индуктивности и электромагнитные излучения, приводящие к искажению формы результирующих импульсов относительно парциальных.

В докладе рассматриваются варианты согласующих сумматоров на основе закрытых двухпроводных линий, свободных от вышеуказанного недостатка, которые обеспечивают сложение парциальных импульсов в режиме бегущих ТЕМ-волн, пакетами которых можно заменить импульсы распространяющиеся по двухпроводным линиям. Для реализации сумматоров используются соединения коаксиальных и радиально-коаксиальных Т-образных тройников, с приминением вложенного и/или последовательного их сопряжения. Возникающие в процессе соединения ненужные каналы связи, по которым могут протекать шунтирующие (паразитные) токи, блокируются с помощью кольцевых магнитопроводов, создающих индуктивно-резистивную развязку.

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CURRENT COMPARATOR DESIGN

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The comparator input is presented by the 6bit differential current output DAC added to the differential signal coming from current output shaper. The comparator is to find the larger of these two differential current signals to determine its output state.

Shaper differential output signals are presented in gaussian form and could vary in amplitude from 50 nA up to 4 μA range. DAC DC differential outputs are moved apart at the comparator's input so as to match shapers' range, i.e. from 0 A up to 4 μA on each differential line. Shaper's signals are also biased by 3 μA current (DC offset).

The comparator is to provide the output switching on the counter load in less than 5 ns range and to be minimized in terms of area and current consumption. We have used UMC CMOS MMRF 180 nm process for the application.

Switching effects and interference through supply rails are to be excluded (main restriction), so there should be no significant (more than 200-300 mV) voltage transitions on intermediate comparator structure stages.

As a reference point of design several current comparator basic schemes have been studied from literature sources, including Traff's [1], Bank's [2], Wang's [3], Chasta's [4]. Finally, the high-compliance mirror topology was chosen as most suitable to fit target requirements. The block-diagram of the current comparator is presented in figure 1.

The distinguishing feature of our design is the absence of high voltage transitions on the intermediate amplification stages to suppress the noise on the input from supply

rail and back-propagation. The signal is presented mostly in differential form, so that common mode noise contributions are mutually subtracted.

This solution however needs tight control over each essential parameter in the schematic by negative feedback paths so that the chip area grows larger. To increase the gain of the converter gain-boosting was used. The description of each block are presented in full version of this work.

Cadence Virtuoso environment was used and the design process was comprised of several steps namely: schematic design, corner analyses and Monte-Carlo modeling, layout, parasitic parameters extraction and verification processes.

The circuit was tested over following corner conditions: power supply variation (1.6 V – 2 V), temperature (0-80 °C), technology variation (ss, tt, ff, fnsp, fpsn).

The total area requirements for the design are 100 µm by 50 µm. The total current consumption is not more than 40 µA over all variations.

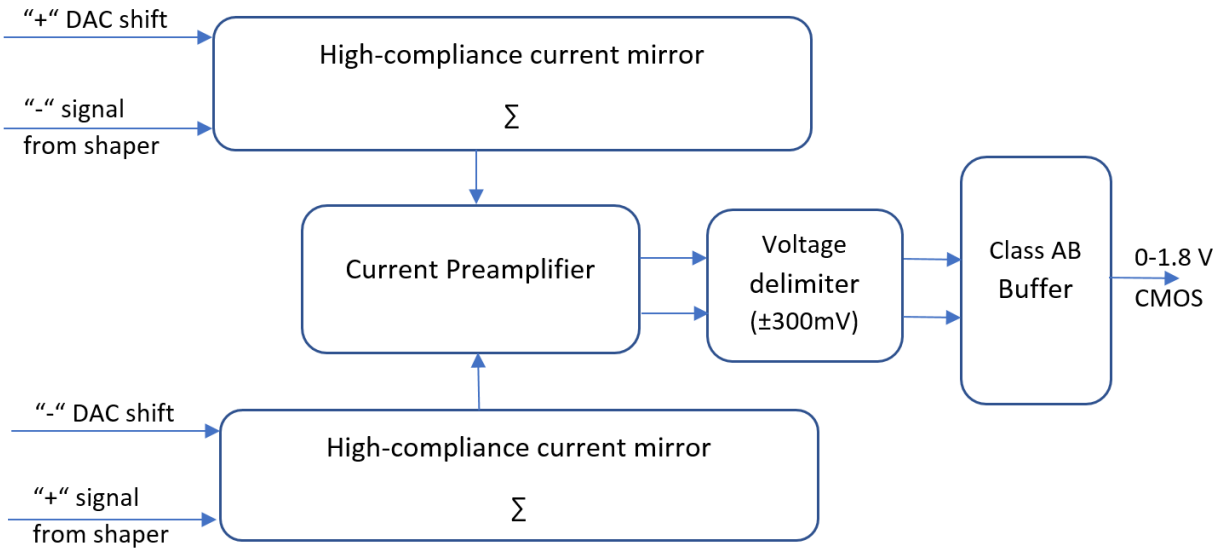

Fig. 1. Block diagram of current comparator

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4. N.K. Chasta. International Journal of VLSI Design & Communication Systems (VLSICS), **3**, №1, 85-96 (2012)